REMARKS

Upon entry of this response, claims 1-4, 6, 10, and 12-20 will be amended. No new matter has been added. These changes have been made solely to expedite prosecution of the current application, and Applicants reserve the right to pursue the subject matter of the originally filed claims in this application and/or other applications. Reconsideration and further examination are respectfully requested.

Specification

The disclosure is objected to because of the following informalities:

-   The abstract is not sufficient because it does not give enough of a description of the present invention.
-   There is no "Brief Summary of the Invention."
-   Requesting agent 210 is referred to as "requesting agent 310" on page 4 line 7 of the specification.

Applicants have amended the abstract and page 4, line 7 of the specification in view of the Examiner's helpful comments.

Applicants request reconsideration of the Examiner's objection to the lack of a "Brief Summary of the Invention." Applicants respectfully suggest that such a section is not mandatory and would not be helpful in the present application.

Claim Rejections – 35 USC § 102

Claims 1-5 and 7-21 are rejected under 35 USC § 102 as being anticipated by Edirisooriya et al. U.S. Patent Application No. 2004/0128450 (hereinafter Edirisooriya).

A brief description of some embodiments claimed herein will be provided with respect to FIG. 6 of the present application. Note, however, that any embodiments claimed herein could be applied to other FIGS.

FIG. 6 illustrates a system 600 with N processors 610, 620, 630 that each may receive IO traffic directly (e.g., not from system memory 650) in a local cache 612, 622, 632.

As applied to claim 1 as amended, a first processor 610 may act as a "requesting agent processor." Moreover, the requesting agent processor 610 may determine that IO traffic should be received directly at the cache 622 of another processor (referred to in claim 1 as a "target processor cache"). That is, processor 610 arranges for IO traffic to be received directly by the cache 622 of a different processor 620.

Applicants respectfully suggest that Edirisooriya does not disclose or suggest such a feature. Referring to FIG. 1 of Edirisooriya, a multi-processor system is disclosed (12a, 12b, 12c). Moreover, a non-processor agent (20a or 20b) may push information directly into processor caches (14a, 14b, or 14c). It does not disclose, however, that one of the processors 12a, 12b, 12c may arrange for information to be routed to a different processor 12a, 12b, 12c.[1]

Nor is such a feature obvious in view of Edirisooriya. For example, because a requesting agent processor might control when and/or how IO traffic is processed, some embodiments may provide flexible approaches applicable to different types of multi-processor systems (Specification at page 5, lines 3-6).

With the exception of claims 15-17, the other pending claims include similar limitations and Applicants respectfully request allowance of the claims.

Claim 15 may be associated with, for example, the embodiment described beginning at page 9, line 5 of the present application. Note that such an embodiment does not need to be directed to a multi-processor system. Applicants respectfully suggest that the references do not disclose or suggest a processing element that arranges for IO traffic to be transferred directly into a destination in accordance with routing information, wherein the destination may be associated with "a system memory for one type of IO traffic and with a processor cache for another type of IO traffic" as recited in claim 15. Thus, Applicants also request allowance of claims 15-17.

---

[1] Applicants note that FIG. 2 of Edirisooriya is a method performed by each processor 12a, 12b, 12c to maintain cache coherency. The method does not determine which processor should receive the information. That determination is instead made by the non-processor agents 20a, 20b.

CONCLUSION

Accordingly, Applicants respectfully request allowance of the pending claims. If any issues remain, or if the Examiner has any further suggestions for expediting allowance of the present application, the Examiner is kindly invited to contact the undersigned via telephone at (203) 972-0191.

Respectfully submitted,

April 17, 2006
Date

Patrick J. Buckley
Registration No. 40,928
Buckley, Maschoff & Talwalkar LLC
Attorneys for Intel Corporation
Five Elm Street
New Canaan, CT 06840
(203) 972-0191